



## Press Release

### **Axilica and SELEX Galileo Collaborate on a new Methodology for Advanced Product Development**

**Loughborough, U.K.** – 26 April 2010. Axilica Limited announced today that SELEX Galileo Ltd has selected Axilica's FalconML as an enabling technology for aspects of an innovative UML-based embedded systems development methodology, which will offer a model-driven approach for the rapid development and enhanced through-life support of EW systems.

SELEX Galileo Ltd (Luton, U.K.), a Finmeccanica Company, is a leader in defence electronics, a key supplier to major military programmes and a provider of integrated sensor solutions and through life capability management for defence systems and homeland security applications. SELEX Galileo's products are designed for inclusion in long-life projects where system capabilities and features must be simple to upgrade and/or ported to support new platforms as underlying technologies evolve during the lifetime of a major project.

"Obsolescence management is a key factor in all our product development projects and determines the methodologies that we adopt for embedded system development spanning both hardware and software," explained Graham Brown, SELEX Galileo Hardware Technical Consultant. "We are using SysML® and UML® modelling to bring together system engineering, software development and hardware development. Axilica's product, FalconML, provides us with a unique capability that enables us to maximise the benefits of this new approach as we are now able to directly generate complex FPGAs from the behavioural descriptions captured in UML models. With FalconML we are able to explore different hardware-software implementations and rapidly deliver hardware prototypes that support the reliable development of the complex embedded software required in our products."

This new development methodology demonstrated by SELEX Galileo captures hardware behaviour and functionality in industry-standard UML modelling tools. FalconML's unique behavioural synthesis engine is used to synthesise these UML models directly into full VHDL or Verilog RTL descriptions, ready for synthesis using traditional hardware development methods and tools. SELEX Galileo benefits from the competitive advantage delivered by FalconML, including

- Focusing hardware modelling on higher levels of abstraction than those supported by traditional RTL-level hardware development. Models capture system behaviour and functionality with resolution of the detailed hardware implementation being performed by FalconML;
- Rapid development of fully functional hardware prototypes which become available early in the system development, supporting detailed software development and, therefore, reducing design iterations, development timescales and overall product development costs; and
- Fast response to changes in customer requirements, changes in deployment platforms (adoption of new hardware) and to software upgrades required during product lifetime.

*(continued overleaf)*



Suresh Radia, Axilica's CEO, commented, "We are delighted to be working with SELEX Galileo in delivering the advanced capabilities needed to support SELEX Galileo's business. FalconML is a unique product that links UML system modelling with existing hardware development methodologies. We expect to continue collaborating with key customers like SELEX Galileo to ensure that FalconML implements hardware-software co-design and hardware synthesis capabilities required for the development of complex embedded systems."

### **About Axilica**

Axilica Limited, which was created by IPSO Ventures plc, is a privately held company with headquarters in Loughborough, U.K. The company is focused on the development of leading-edge behavioural synthesis solutions for the deployment of complex embedded systems.

The company's product, FalconML, enables the use of industry-standard SysML and UML modelling tools for the implementation of complex hardware devices, such as FPGAs and ASICs, within advanced embedded systems. FalconML synthesises UML models providing options for hardware-software co-design; for generation of SystemC descriptions for fast system simulation; and for the generation of an RTL description in VHDL or Verilog for subsequent synthesis to a gate-level description.

For further information on Axilica or any of its products, please visit [www.axilica.com](http://www.axilica.com), call +44 (0)1509 227131 or email [info@axilica.com](mailto:info@axilica.com).

SysML and UML are registered trademarks of the OMG Group.