



## Press Release

### **Axilica secures 495K grant from European Commission FP7 program to enhance FalconML to support MARTE and multi-core processors**

**Loughborough, U.K.** – 26 April 2010. Axilica Limited announced today that in partnership with other European companies - including Thales Communications, Softeam (France); Loughborough University (UK); and University of Peloponnese and Intracom (Greece) - it has secured a total grant of 2.6M from the European Commission FP7 program for the ENOSYS project (**intEgrated modelliNg and synthesis tOol flow for embedded SYStems design**).

Axilica has received 495K to enhance its product, FalconML, to provide core synthesis technology linking MARTE modelling, deployment on multi-core processors and innovative direct C synthesis that form part of the ENOSYS design flow.

Suresh Radia, Axilica's CEO, commented, "We are delighted to be working with our partners to develop a state of art design environment for hardware/software co-design which integrates high-level system modelling with MARTE, software code generation, hardware synthesis and design space exploration." Suresh added, "The ENOSYS integrated tool chain addresses key challenges in the development of complex silicon processing platforms and Axilica is delighted to have been selected to provide the core synthesis engine for the project."

ENOSYS will develop and validate an integrated workbench with specific scientific and technological objectives that include:

- Development of MARTE extensions that address the needs for capturing high level specifications and for design synthesis;
- Integration of the MARTE profile into the existing tool flow, permitting the automatic generation of SystemC and hardware synthesis into HDL;
- Developing the means for the rapid and automated determination of near-optimal embedded system implementations using design space exploration techniques; and
- Development of the tool support required for seamless software/hardware co-design.

#### **About ENOSYS – FP7**

The ENOSYS project is funded under the European Commission's Seventh Framework Programme, which is the European Union's main mechanism for funding and encouraging leading edge research and technological development. ENOSYS aims to shorten time to market and to reduce design costs in the development of new electronic products. This is of prime importance to European companies seeking to increase their share of the competitive consumer electronics market, where the flexibility to move quickly to add distinguishing features, such as faster operation, lower power consumption or miniaturization, is paramount.

For further information on ENOSYS, please visit [www.enosys-project.eu/enosys-project](http://www.enosys-project.eu/enosys-project)

*(continued overleaf)*



## **About Axilica**

Axilica Limited, which was created by IPSO Ventures plc, is a privately held company with headquarters in Loughborough, U.K. The company is focused on the development of leading-edge behavioural synthesis solutions for the deployment of complex embedded systems.

The company's product, FalconML, enables the use of industry-standard SysML and UML modelling tools for the implementation of complex hardware devices, such as FPGAs and ASICs, within advanced embedded systems. FalconML synthesises UML models providing options for hardware-software co-design; for generation of SystemC descriptions for fast system simulation; and for the generation of an RTL description in VHDL or Verilog for subsequent synthesis to a gate-level description.

For further information on Axilica or any of its products, please visit [www.axilica.com](http://www.axilica.com), call +44 (0)1509 227131 or email [info@axilica.com](mailto:info@axilica.com).

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